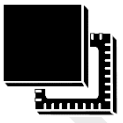
SPM1173 Datasheet

32-bit ARM Cortex-M4 based MCU with 7 channel 14-bit ADC, integrated 600V high voltage gate driver and power MOS module

Features

- ARM 32-bit Cortex-M4 CPU Core with FPU
  - 100 MHz maximum frequency
- Memories
  - Up to 64 KB embedded flash
  - Up to 32 KB RAM
- Clock, reset and supply management
  - 3.3 V DVDD and 15V VDDG power supply
  - POR, Brown-out detector (BOD)
  - 1 ~ 66 MHz external crystal oscillator
  - Internal 32 MHz factory-trimmed oscillator
  - Internal 2.2MHz backup-safety oscillator
  - PLL for CPU clock
- 14-bit A/D converters (up to 8 channels)
  - As low as 140 ns conversion time
  - Conversion range: 0 to 3.65 V
  - Differential sample
  - Triple-sample and hold capability
  - Open/short detection for safety
  - Temperature sensor
- Analog comparator
  - 7 high-speed comparators
  - Output with digital deglitch filter
  - Four DACs as reference
  - Out of range voltage protection
  - Phase comparison
- PWM



HFBP39 (12 × 12 × 0.75 mm^3)

  - Flexible waveform generation with phase lead/lag control
  - All events can trigger ADC conversion
- Up to 12 GPIO Pins
  - Configurable pull-up/pull-down resistors
  - Programmable digital input deglitch filter
- Enhanced Capture Module (ECAP)
  - Flexible input capture pin
  - Four 32-bit capture registers
  - Capture and APWM mode selection
- Debug mode
  - Serial wire debug (SWD) & JTAG interfaces
- Communication interfaces
  - UART x 1, SIO x 1
  - SIO can be configured as UART.
- Security Modules
  - CRC x 1, AES x 1, 64-bit unique ID
- Operating temperature
  - Junction temperature: -40 to +125 °C
  - Ambient temperature: -40 to +105 °C
- High voltage module
  - 3 phase 600V pre-drivers
  - 6 integrated MOS

Peripherals	SPM1173API39
Flash	64 KB
OTP Flash	512 byte
SRAM	32 KB
GPIOs[1]	12
14-bit ADC channel	1 7 external input channel
COMP	7
DAC	4
PWM channel	1 2 channel
ECAP	1
GPT	3
WDT	2
AES	1
CRC	1
UART	1
SIO	1
CPU max frequency	100 MHz

[1] The GPIO40 (ISP) pin is not included.

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Revision history

Version	Date	Author	Status	Changes
0	2022-07-08	–	Outdated	1. Draft.
A/0	2023-03-01	–	Outdated	1. Update ADC characteristic. 2. Update Table 6-1. 3. Update Section 1.
A/1	2023-03-03	–	Outdated	1. Update Table 3-1, Figure 3-1.
A/2	2023-11-29	–	Outdated	1. Update Figure 6-1, Table 6-1. 2. Update IO information, MCU related SPEC.
A/3	2024-04-04	–	Outdated	1. Update package information, Power MOS information.
C/0	2025-02-14	J. Zhou	Outdated	1. Adjust the document format. 2. Modify Table 6-1. 3. Modify Table 8-1.
C/1	2025-06-10	J. Zhou	Released	1. Modify Table 5-13 and Table 5-14. 2. Modify fRCO in Table 5-4. 3. Add ∑IOH and ∑IOL in Table 5-3. 4. Add power-up slope of DVDD and VDDG in Table 5-2. 5. Change the signal name of pin 9 to VCAP12A. Change the signal name of pin 33 to VCAP12B. 6. Correct the description of peripheral devices. 7. Add Section 5.16 and 5.17.

Terms or abbreviations

Terms or abbreviations	Description
MCU	Microcontroller Unit
LDO	Low Dropout Regulator
BLDC	Brushless Direct Current
FET	Field Effect Transistor

1 Device overview

The SPM1173 device from Spintrol is a highly integrated system-on-chip (SiP) microcontroller. As shown in Figure 1-1, The SPM1173 incorporates a 32-bit ARM Cortex-M4 high-performance processor with a software-programmable clock rate as high as 100 MHz, 32 KB SRAM, embedded flash with 64 KB, and an extensive range of enhanced I/Os and peripherals. The device offers a 14-bit ADC, enhanced PWMs, three general purpose 32-bit timers, as well as standard and advanced communication interface: UART. Meanwhile, this device also includes a high voltage three-phase gate driver and 6 power MOS to serve as a module to directly drive BLDC motor. To save board area, bootstrap diode is also integrated in the gate driver. The high voltage MOS has DC current rating of 2A. These features make the SPM1173 ideal for motor control application.

The SPM1173 operates from a 2.97 ~ 3.63 V DVDD power supply, with VBUS voltage up to 600V, VDDG is used to define the gate-source voltage swing for power MOS, usually 15V. The temperature range is from -40 °C to +125 °C. The package type is 39-pin HFBP.

Figure 1-1 shows the typical application block diagram of SPM1173. Figure 1-2 shows the functional diagram for the SPM1173. Figure 1-3 shows the clock tree information.

Figure 1-1: SPM1173 Typical application diagram

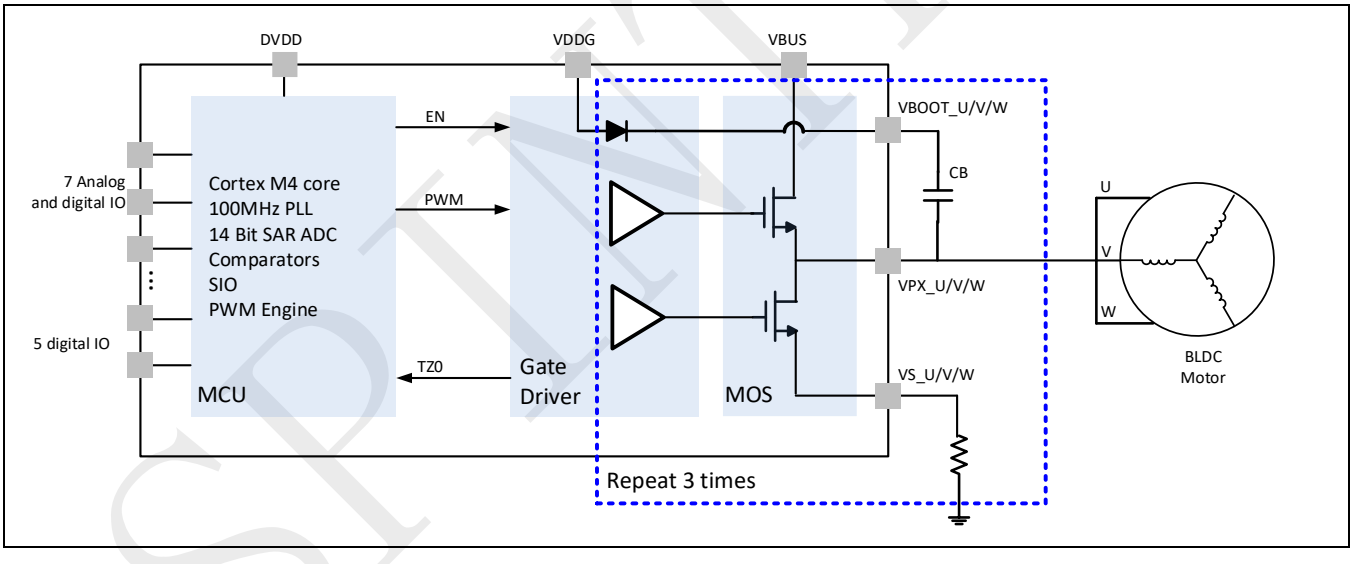


Figure 1-2: SPM1173 System Function Diagram

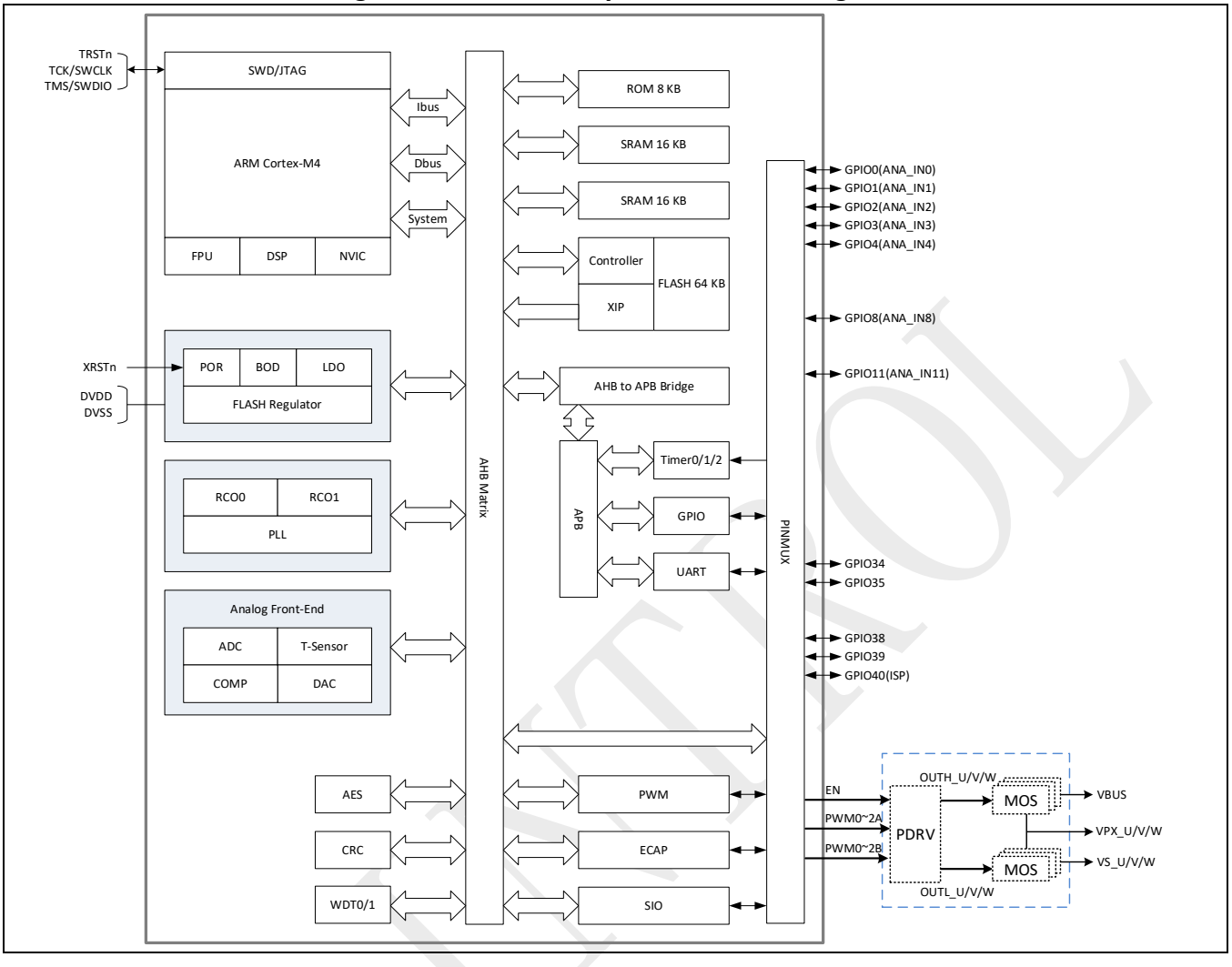
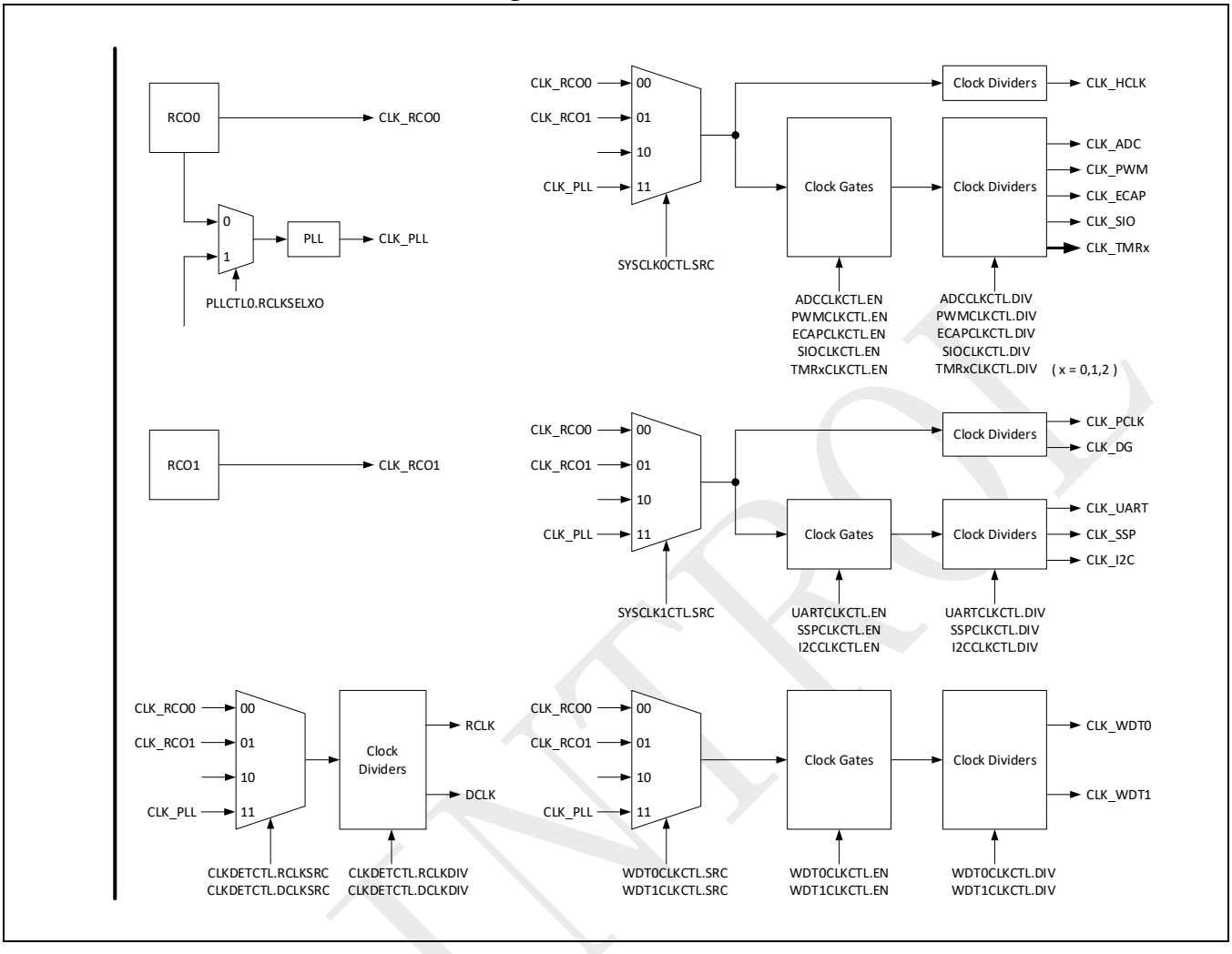


Figure 1-3: Clock tree



2 Feature descriptions

2.1 ARM Cortex-M4 core

The ARM Cortex-M4 processor has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The SPD1163 integrates a full-feature ARM Cortex-M4 core with FPU that can run up to 100MHz. Therefore, it is compatible with all ARM tools and software.

2.2 Embedded SRAM

The SPM1173 has implemented 32 KB SRAM memory for code and data. The SRAM can be accessed (read/write) at CPU clock speed with 0 wait states.

2.3 Embedded Flash memory

Up to 64 KB of embedded Flash memory is available for storing programs and data. To enhance the lifetime and store critical data, another 12 KB Flash memory is used for EEPROM emulation to support up to 1 KB effective capacity.

2.4 Nested vectored interrupt controller (NVIC)

The SPM1173 embeds a nested vectored interrupt controller able to handle up to 51 mask-able interrupt channels (not including the 16 interrupt-lines of Cortex-M4) and 16 programmable priority levels.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Support for lazy-stacking
- Interrupt entry restored on interrupt exit with no instruction overhead

2.5 External interrupt/event controller

The SPM1173 provides a flexible external pin interrupt or event trigger mechanism. Any GPIO pin can be programmed as an external interrupt or event trigger source. In addition, any GPIO interrupt can be configured as edge-triggered or level-triggered.

2.6 Power supply and reset

The SPM1173 supports 3.3V DVDD and 15V VDDG power supplies, providing power for IO, internal voltage regulators and on-chip analog circuits. It is important to note that the boost rate of the DVDD power supply is less than or equal to 0.015 V/us.

The SPM1173 has a global reset pin as well as an integrated power-on reset (POR) circuitry. The POR circuitry guarantees all power-up reset sequence requirements and makes the device easy to use.

2.7 Brown-out detector

The device features an embedded brown-out detector (BOD) that monitors the 3.3V/1.2V domain power supply and compare it to the programmable pre-set value. An interrupt or reset can be generate when voltage of the power domain is higher or drops below the pre-set value. The interrupt service routine then generates a warning message and/or put the MCU into a safe state. The BOD is enabled by software.

2.8 Clocks

System clock selection is performed on startup. The internal 32 MHz factory-trimmed oscillator is selected by default upon reset. An external oscillator can be selected by the user.

The device implements a fractional phase-lock loop (PLL) for high frequency clock generation. The PLL can take the internal 32 MHz oscillator or external clock as the input reference clock. The output frequency covers from 25 MHz to 100 MHz.

Several clock dividers allow the configuration of the AHB, and the peripherals frequency. The maximum allowed frequency is s 100 MHz for AHB and 50 MHz for APB. See Figure 1-3 for details on the clock tree. Special clock selection logic is designed so that the backup clock can take charge if current clock is missing. The 2.2 MHz backup-safety oscillator makes the SPM1173 get rid of clock stuck.

2.9 Boot mode

The boot code is located in on-chip ROM memory. After reset, the ARM processor starts code execution from the ROM. The ISP pin(GPIO40) and TRSTn pin are used to select one of the two boot options:

- Boot from embedded Flash (ISP pin = 1, TRSTn pin = X): the boot loader jumps to the embedded Flash and runs from the address at 0x1000 0000
- ISP mode (ISP pin = 0, TRSTn pin = 0): the boot loader reprograms the embedded Flash by using UART. During the process, the GPIO34 is configured as UART_TXD and the GPIO35 is configured as UART_RXD.

Note: The TRSTn pin is recommended to set as low.

2.10 General-purpose IOs (GPIOs)

The SPM1173 can be configured to support as many as 12 multi-purpose GPIO pins. Each GPIO pin can be configured by software as input, as output or as peripheral alternate function. It features:

- Each GPIO pin has configurable internal pull-up and pull-down resistors.
- Each GPIO pin has a programmable digital input deglitch filter.
- Pure 3.3V I/O capability multiplexed with ADC input channel for GPIO0~GPIO4/GPIO8/GPIO11.

2.11 Timers and watchdogs

The SPM1173 device includes three general-purpose timers, two watchdog timers and a SysTick timer.

General-purpose timers

The SPM1173 includes three identical 32-bit general-purpose timers. Each general-purpose timer consists of a 32-bit auto-reload down-counter. An interrupt would be generated when the counter reaches zero if it is enabled. When the counter reaches zero, the timer can also generate an ADCSOC event or a PWMSYNC event if they are enabled. The clock of general-purpose timer can be selected from internal RC oscillators, external oscillator or PLL clock. Besides, each general-purpose timer can also be configured to use external pin as enable control, event for the counter, or event to capture current counter value.

Watchdogs

The SPM1173 implements two identical watchdogs. Each watchdog is based on a 32-bit down-counter, which can be clocked from internal RC oscillators, external oscillator or PLL clock. When the counter reaches the given time-out value, an interrupt or a reset can be generated. The watchdog counter can be frozen or free-running in debug mode.

SysTick Timer

This timer is dedicated for the operating system, but could also be used as a standard down-counter. It features:

- A 24-bit down-counter.
- Auto-reload capability.
- Mask-able system interrupt generation when the counter reaches 0.

2.12 UART

The SPM1173 has one UART module that features:

- Ability to add or delete standard asynchronous communication bits (start, stop and parity) in the serial data.

- 5 – 8 data bits.
- Even, odd or no parity detection.
- One, one-and-a-half, or two stop bits generation.
- Baud-rate generation up to 6.25 Mbps.
- 64-byte transmit FIFO.
- 64-byte receive FIFO.
- Auto baud-rate detection.

2.13 ADC

SPM1173 is equipped with a 14-bit analog-to-digital converter with 7 external input channels. Temperature sensors, internal power supplies, etc. can be used as the input of the analog-to-digital converter through multiplexing. The core of this analog-to-digital converter contains 3 independent sample-and-hold circuits, and each sample-and-hold circuit has 2 input channels, which are suitable for differential sampling.

Events generated by the general timer and the pulse width modulation output can both trigger the start of the analog-to-digital converter.

- 14-bit resolution.
- Minimum 140 ns conversion time and independently configurable sampling time.
- Differential sampling.
- 3-channel sampling hold.
- Supports synchronous sampling and serial sampling.
- Analog signal input range: 0 V ~ 3.65 V.
- Option for internal or external reference voltage.
- Input open circuit and short circuit detection.

Please see Table 5-8 for 14-bit ADC characteristics.

2.14 Temperature sensor

The temperature sensor generates a voltage that varies linearly with temperature. It is internally connected to the ADC input channel, which is used to convert the sensor output voltage into a digital value.

2.15 Analog comparators

The SPM1173 is equipped with 7 high-speed comparators. Each comparator uses the internal digital-to-analog converter (DAC) as the reference to monitor whether the input or output of the programmable gain amplifier exceeds the threshold. The DAC can be used to generate a static voltage as the threshold for the comparator, but it does not guarantee the performance of generating waveforms by dynamically changing the code value. The output of the comparator is connected to the Pulse Width Modulation Trip-Zone module. Additionally, each comparator can achieve the function of phase comparison, which can be used for the detection of motor commutation. For specific channel selection details, please refer to the technical reference manual of the chip.

- 50 ns typical response.
- Programmable hysteresis.
- Output with digital deglitch filter.
- Phase comparison function.

For more details on the characteristics of analog comparators and digital analog converters, please refer to Table 5-9 and Table 5-10.

2.16 PWMs

The SPM1173 integrates supports two PWM channels. Without much involvement of processor core, PWM can generate complex pulse width waveforms.

- Dedicated 16-bit time-base counter with period and frequency control.
- Two outputs with single-edge operation, dual-edge symmetric operation or dual-edge asymmetric operation.
- All events can trigger both CPU interrupts and ADC start of conversion.
- Programmable phase-control support for lag or lead operation relative to other PWM modules.
- Dead-band generation with independent rising and falling edge delay control.
- Programmable trip zone allocation of both cycle-by-cycle trip and one-shot trip on fault conditions.
- A blocking condition can force either high, low, or high-impedance state logic levels at PWM outputs.
- Comparator module outputs and trip zone inputs can generate events, filtered events, or trip conditions.

2.17 ECAP

The SPM1173 has implemented an ECAP module with following features:

- Flexible input capture pin: each GPIO can be configured as capture pin
- 32-bit time base counter
- 4 x 32-bit time-stamp capture registers
- 4-stage sequencer that is synchronized to external events
- Independent edge polarity (rising/falling edge) selection for all 4 events
- Interrupt capabilities on any of the 4 capture events

2.18 Cyclic redundancy check (CRC)

The SPM1173 has a hardware CRC calculation unit. The CRC module is used to verify data transmission or storage integrity. It features:

- 32-bit parallel bit stream input, and up to 32-bit CRC output.
- Support up to 2^{32} byte length for CRC calculation.
- FIve CRC standard polynomials supported.

2.19 Advanced Encryption Standard Engine (AES)

AES module provides fast hardware encryption and decryption services. Its main features are as follows:

- Supports up to 6 block encryption modes: ECB, CBC, CTR, CCM*, MMO, and Bypass.
- Supports 128-bit, 192-bit, and 256-bit keys.
- Each block encryption mode has error indication.
- Independent 4 x 32-bit input and output first-in-first-out queues.

2.20 Serial wire JTAG debug port (SWJ-DP)

The built-in ARM SWJ-DP interface is composed of JTAG and serial line debugging ports. Based on the SWJ-DP interface, a serial line debugging probe or JTAG probe can be connected to the target. When SPM1173 enables certain security functions, the debugging ports can be disabled.

2.21 SIO

SPM1173 is equipped with one SIO module, which is a patented technology of Spintrol. This SIO module can be programmed to be configured as the communication module pre-defined by the user. Currently, through initialization settings, the SIO can be configured for functions such as UART.

2.22 3-Phase Pre-Driver

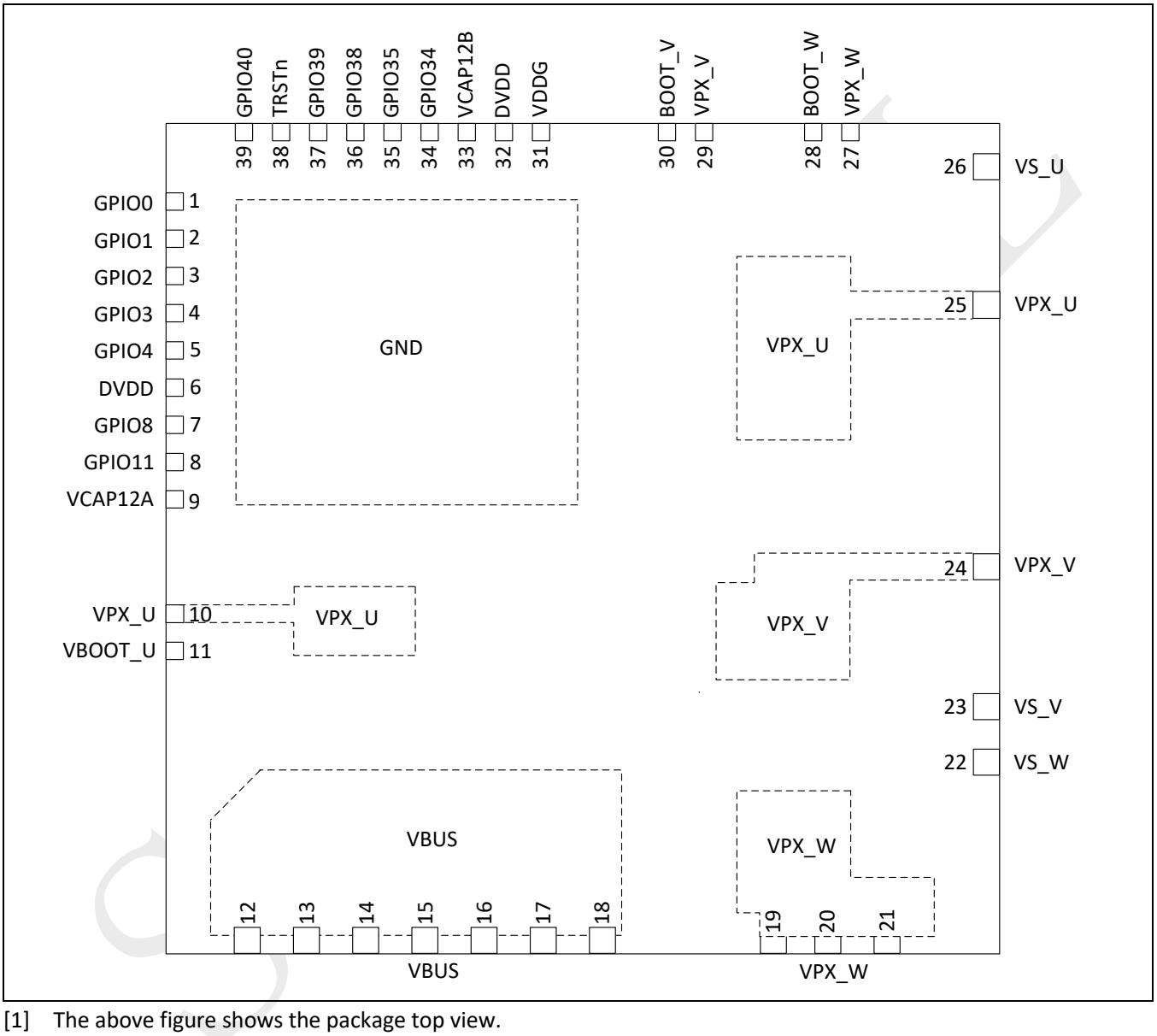
SPM1173 integrates six high-voltage high-speed power MOSFETs and drivers, providing three independent high and low-side reference output channels, suitable for three-phase applications.

- Fault detection: Provides a FAULT signal to indicate the trigger state of undervoltage shutdown.
- Integrated 6 channels of MOSFETs, with a conduction resistance of 1.9Ω and a current of 2A.
- Delay matching: The propagation delay has been optimized through matching to facilitate the design of high-frequency applications.
- Dead-time control: Built-in dead-time (typical value 300ns), preventing the high and low-side MOSFETs from conducting simultaneously.
- Pre-driving logic integrated noise filter, which can filter out input logic pulses with a pulse width less than 270ns, enhancing the system's anti-interference capability.

3 Pinouts and pin description

3.1 HFBP39

Figure 3-1: SPM1173 HFBP39 pinout



[1] The above figure shows the package top view.

[2] Note: there is no need to connect the two VCAP12 pins on the PCB boards.

[3] Note: when TRSTn is HIGH, GPIO38 ~ GPIO39 pins work as Debug interface and can't be configured as other functions.

Table 3-1: SPM1173 HFBP39 pin definitions

Pin	Signal	Type[1]	Description
1	GPIO0	I/O	General-purpose input/output 0
	ANA_IN0	AI	ADC channel 0 input
	COMP0H	O	Comparator COMP0H result output
2	GPIO1	I/O	General-purpose input/output 1
	ANA_IN1	AI	ADC channel 1 input
	COMP0L	O	Comparator COMP0L result output
3	GPIO2	I/O	General-purpose input/output 2
	ANA_IN2	AI	ADC channel 2 input
	COMP1H	O	Comparator COMP1H result output
4	GPIO3	I/O	General-purpose input/output 3
	ANA_IN3	AI	ADC channel 3 input
	COMP1L	O	Comparator COMP1L result output
5	GPIO4	I/O	General-purpose input/output 4
	ANA_IN4	AI	ADC channel 4 input
	COMP2H	O	Comparator COMP2H result output
6	DVDD	S	3.3V power, **add 4.7uF and 0.1uF bypass ceramic cap to AVSS**
7	GPIO8	I/O	General-purpose input/output 8
	ANA_IN8	AI	ADC channel 8 input
	COMP3H	O	Comparator COMP3H result output
8	GPIO11	I/O	General-purpose input/output 11
	ANA_IN11	AI	ADC channel 11 input
	COMP4L	O	Comparator COMP4L result output
9	VCAP12A	S	1.2V power, **add 2.2uF and 0.1uF bypass ceramic cap to DVSS**
10	VPX_U	S	U Phase high side supply offset voltage
11	VBOOT_U	S	U Phase high side power
12/13/14/15/16/17/18	VBUS	S	Supply voltage
19/20/21	VPX_W	S	W Phase motor driving out
22	VS_W	S	W phase driver GND
23	VS_V	S	V phase driver GND
24	VPX_V	S	V Phase motor driving out
25	VPX_U	S	U Phase motor driving out
26	VS_U	S	U phase driver GND
27	VPX_W	S	W Phase high side supply offset voltage
28	VBOOT_W	S	W Phase high side power
29	VPX_V	S	V Phase high side supply offset voltage
30	VBOOT_V	S	V Phase high side power
31	VDDG	S	Gate driver power supply
32	DVDD	S	3.3V power, **add 4.7uF and 0.1uF bypass ceramic cap to AVSS**

Pin	Signal	Type[1]	Description
33	VCAP12B	S	1.2V power, **add 0.1uF bypass ceramic cap to DVSS**
34	GPIO34	I/O	General-purpose input/output 34
	UART_TXD	O	UART transmit data
	UART_RXD	I	UART receive data
	SIO0_12	I/O	SIO0 input/output 12
35	GPIO35	I/O	General-purpose input/output 35
	UART_RXD	O	UART receive data
	UART_TXD	I	UART transmit data
	SIO0_13	I/O	SIO0 input/output 13
36	GPIO38	I/O	General-purpose input/output 38
	TMS/SWD	I/O	JTAG mode select or SWD data
	UART_TXD	I	UART transmit data
	PWM2A	O	PWM2 output A
	SIO0_16	I/O	SIO0 input/output 16
	Note: when TRSTn is HIGH, this pin always works as TMS/SWD and can't be configured as other function		
37	GPIO39	I/O	General-purpose input/output 39
	TCK/SWCK	I	JTAG clock or SWD clock
	PWM2B	O	PWM2 output B
	SIO0_17	I/O	SIO0 input/output 17
38	TRSTn	I	JTAG reset pin, reset the JTAG when low
39	ISP(GPIO40)	I/O	ISP pin (General-purpose input/output 40)
	UART_TXD	O	UART transmit data
	DCLK	O	Clock output from CLKDET module for monitoring
	SIO0_0	I	SIO0 input/output 0

[1] I = digital input, O = digital output, AI = analog input, AO = analog out, S = supply.

[2] All GPIO pins can be configured as ECAP input.

3.2 Connection between the internal MCU and the pre-driver

Table 3-2: Connection between the internal MCU and the pre-driver

MCU pin	Pin configuration	Pre-driver signal description
GPIO28	GPIO output	Enable control of pre-driver
GPIO18	PWM0A	Input of upper PWM waveform for phase W of pre-driver
GPIO19	PWM0B	Input of lower PWM waveform for phase W of pre-driver
GPIO20	PWM1A	Input of upper PWM waveform for phase V of pre-driver
GPIO21	PWM1B	Input of lower PWM waveform for phase V of pre-driver
GPIO22	PWM2A	Input of upper PWM waveform for phase U of pre-driver
GPIO23	PWM2B	Input of lower PWM waveform for phase U of pre-driver

3.3 ADC input channel selection

Table 3-3: ADC input channel selection

Option	SHA		SHB		SHC	
	SELP	SELN	SELP	SELN	SELP	SELN
0	GND		GND		GND	
1	–	–	–	–	–	–
2	DAC0	DAC0	DAC1	DAC1	DAC2	DAC2
3	DVDD	VDD12	ATEST	VDCBUF	TSEN1	TSEN0
4	ANA_IN0	ANA_IN1	ANA_IN0	ANA_IN1	ANA_IN0	ANA_IN1
5	ANA_IN2	ANA_IN3	ANA_IN4	–	–	–
6	ANA_IN8	–	ANA_IN8	–	ANA_IN8	–
7	–	ANA_IN11	–	–	–	–

3.4 Function and Status of the GPIO pins after reset

Table 3-4: Function and status of the GPIO pins after reset

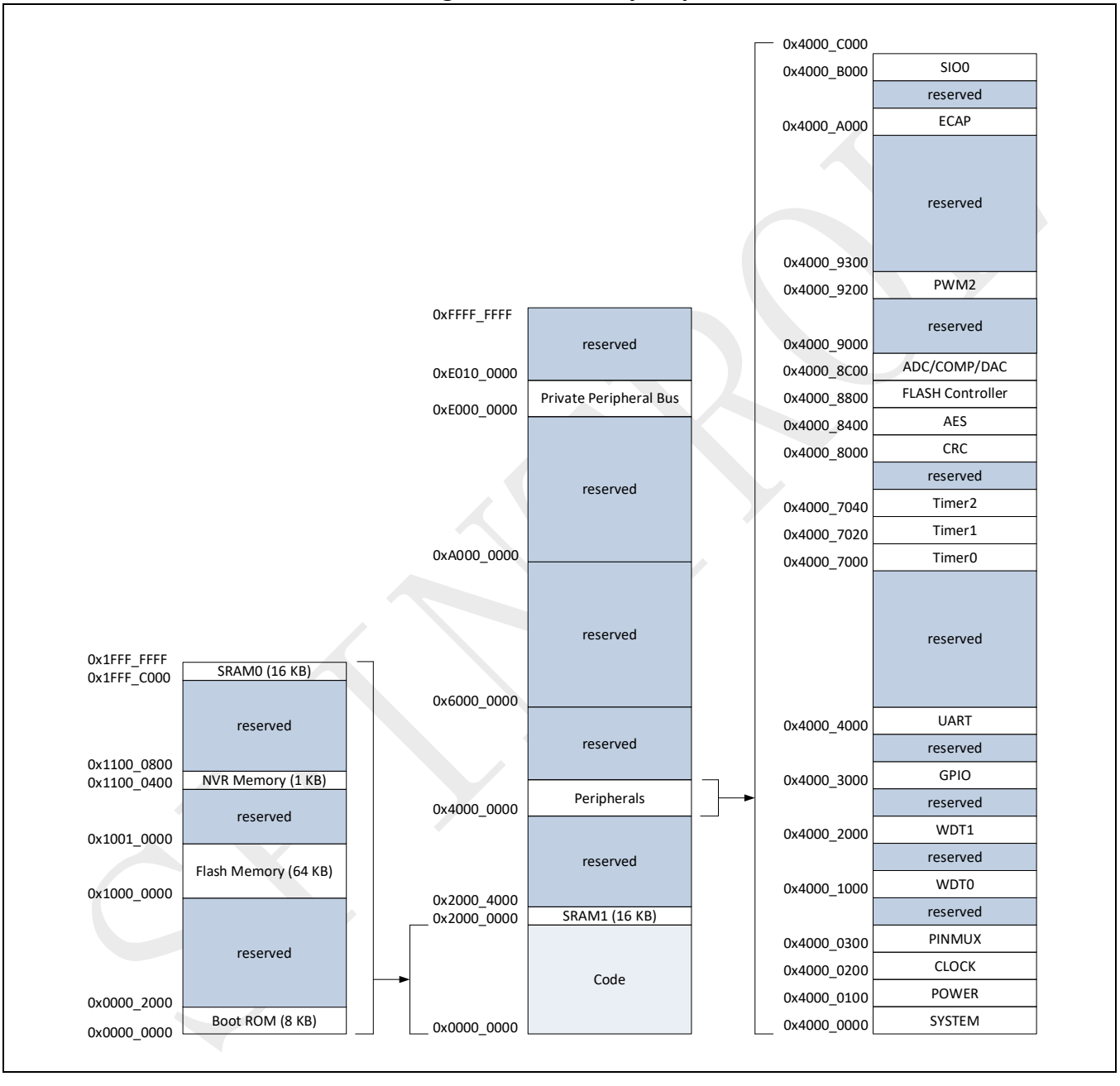
Pin Name	Default Function	Default State
GPIO0	ANA_IN0	Floating
GPIO1	ANA_IN1	Floating
GPIO2	ANA_IN2	Floating
GPIO3	ANA_IN3	Floating
GPIO4	ANA_IN4	Floating
GPIO8	ANA_IN8	Floating
GPIO11	ANA_IN11	Floating
GPIO18[1]	GPIO18	Floating
GPIO19[1]	GPIO19	Floating
GPIO20[1]	GPIO20	Floating
GPIO21[1]	GPIO21	Floating
GPIO22[1]	GPIO22	Floating
GPIO23[1]	GPIO23	Floating
GPIO28[1]	GPIO28	Floating
GPIO34	GPIO34	Pull up
GPIO35	GPIO35	Pull up
GPIO38	GPIO38	Floating
GPIO39	GPIO39	Floating
GPIO40	GPIO40/ISP	Pull up

[1] Internal pin.

4 Memory Map

The memory map of SPM1173 is shown in Figure 4-1.

Figure 4-1: Memory Map



5 Electrical characteristics

5.1 Absolute maximum ratings

Table 5-1: Absolute maximum ratings [1][2]

Symbol	Parameter	Min	Max	Unit
V_{BUS}	High voltage power supply	-0.3	600	V
V_{VDDG}	Pre-Driver power supply	-0.3	22	V
$V_{VPX\_U/V/W}$	High side floating ground	-10	600	V
$V_{VBOOT\_U/V/W}$	High side floating supply	-0.3	622	V
V_{DVDD}	Supply voltage, with respect to V_{SS}	-0.3	4.6	V
V_{IN}	Input voltage (V_{DVDD} = 3.3 V)	-0.3	4.6	V
V_{OUT}	Output voltage	-0.3	4.6	V
I_{IC}	Input clamp current	-20	+20	mA
I_{OC}	Output clamp current	-20	+20	mA
T_J	Junction temperature [3]	-40	+125	°C
T_A	Ambient temperature [3]	-40	+105	°C
T_{stg}	Storage temperature [3]	-65	+150	°C

[1] Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these is not implied.

[2] All voltage values are with respect to VSS, unless otherwise noted.

[3] Long-term high-temperature storage or extended use at maximum temperature conditions may result in a reduction of overall device life.

5.2 Recommended operating conditions

Table 5-2: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Nom	Max	Unit
V_{DVDD}	Power supply voltage	–	2.97	3.3	3.63	V
dV_{DVDD}/dt	External DVDD power-up slope	–	–	–	0.015	V/us
V_{VDDG}	Power supply voltage	–	8.9	15	20	V
dV_{VDDG}/dt	VDDG power-up slope	–	–	–	1	V/us
V_{DVSS}	Power ground (epad)	–	–	0	–	V
V_{IH}	High-level input voltage	V_{DVDD} = 3.3 V	2.0	–	V_{DVDD} + 0.3	V
V_{IL}	Low-level input voltage	V_{DVDD} = 3.3 V	V_{DVSS} - 0.3	–	0.8	V
I_{OH}	High-level output source current when $V_{OH} = V_{OH(MIN)}$	STRENGTH=0 STRENGTH=1 STRENGTH=2 STRENGTH=3	–	–	5 10 15 20	mA
I_{OL}	Low-level output sink current when $V_{OL} = V_{OL(MAX)}$	STRENGTH=0 STRENGTH=1 STRENGTH=2 STRENGTH=3	–	–	5 10 15 20	mA
T_J	Junction temperature	–	-40	–	125	°C
T_A	Ambient temperature	–	-40	–	105	°C

5.3 I/O Electrical characteristics

Table 5-3: I/O Electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	High-level output voltage	I_{OH} = I_{OH} MAX	V_{DVDD} - 0.4	–	–	V
V_{OL}	Low-level output voltage	I_{OL} = I_{OL} MAX	–	–	0.4	V
V_{IH}	High-level input voltage	V_{DVDD} = 3.3 V	2.0	–	V_{DVDD} + 0.3	V
V_{IL}	Low-level input voltage	V_{DVDD} = 3.3 V	V_{DVSS} - 0.3	–	0.8	V
I_{OH}	High-level output source current when V_{OH} = $V_{OH(MIN)}$	STRENGTH=0 STRENGTH=1 STRENGTH=2 STRENGTH=3	–	–	5 10 15 20	mA
I_{OL}	Low-level output sink current when V_{OL} = $V_{OL(MAX)}$	STRENGTH=0 STRENGTH=1 STRENGTH=2 STRENGTH=3	–	–	5 10 15 20	mA
I_{IL}	Low-level input current (Pin with pull-up and pull-down disabled)	V_{DVDD} = 3.3V V_{IH} = 0 V	–	–	2	uA
I_{IH}	High-level input current (Pin with pull-up and pull-down disabled)	V_{DVDD} = 3.3V V_{IH} = V_{DVDD}	–	–	2	uA
$\sum I_{OH}$	Total current of each group of I/O output sources [1]	–	–	–	80	mA
$\sum I_{OL}$	Total current of each group of I/O input sinking currents [1]	–	–	–	80	mA
R_{PU}	Input pull-up resistor	V_{IO} = 0 V	–	41	–	kΩ
R_{PD}	Input pull-down resistor	V_{IO} = V_{DVDD}	–	42	–	kΩ

[1] The I/O between two adjacent 3.3V power supply pins constitutes one group.

5.4 RCO characteristics

Table 5-4: RCO characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DVDD}	3.3V power supply	–	2.97	3.3	3.63	V
f_{RCO}	RCO frequency at room temperature	T_J = 25 °C	31.936	–	32.064	MHz
ACC_{RCO}	RCO frequency accuracy (RCO frequency variation versus temperature)	T_J = -40~150 °C	-1	–	1	%
t_{RDY}	RCO frequency ready time	–	–	4.2	–	us

5.5 Internal 1.2V Voltage Regulator characteristics

Table 5-5: Internal 1.2V Voltage Regulator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DVDD}	Power supply	–	2.97	3.3	3.63	V
VCAP12	Output voltage	Load current = 50mA	1.18	1.20	1.22	V
ΔVCAP12	Load regulation rate	VCAP12 (L = 50mA) - VCAP12 (L = 200mA)	–	–	30	mV

Figure 5-1: Internal 1.2V voltage regulator load regulation rate (T_A = 25 °C)

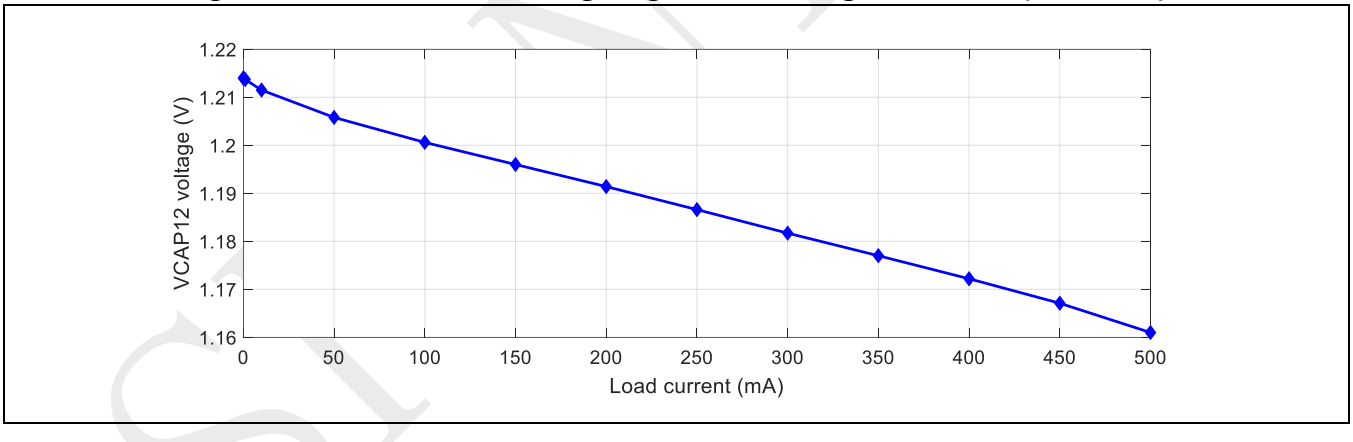
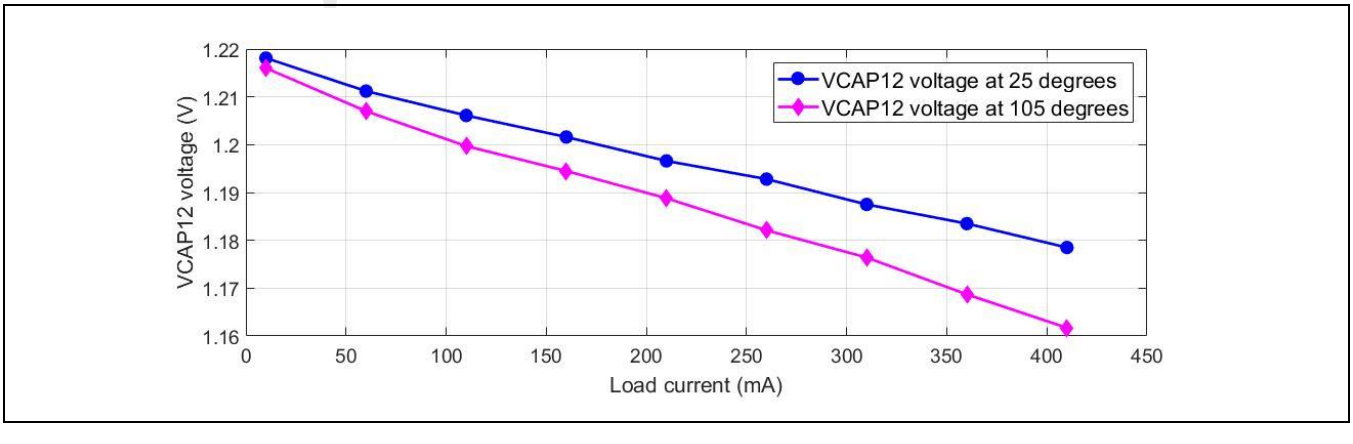


Figure 5-2: Internal 1.2V Regulator Load Regulation vs. Temperature



5.6 BOD characteristics

Table 5-6: BOD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DVDD}	3.3V power supply	–	2.97	3.3	3.63	V
$V_{DVDDOV,assert}$	VDD33 over-voltage assert threshold	–	–	3.42	–	V
$V_{DVDDOV,release}$	VDD33 over-voltage release threshold	–	–	3.31	–	V
$V_{DVDDUV,assert}$	VDD33 under-voltage assert threshold	–	–	2.58	–	V
$V_{DVDDUV,release}$	VDD33 under-voltage release threshold	–	–	2.65	–	V
$V_{VCAP12OV,assert}$	VDD12 over-voltage assert threshold	–	–	1.33	–	V
$V_{VCAP12OV,release}$	VDD12 over-voltage release threshold	–	–	1.31	–	V
$V_{VCAP12UV,assert}$	VDD12 under-voltage assert threshold	–	–	0.94	–	V
$V_{VCAP12UV,release}$	VDD12 under-voltage release threshold	–	–	0.97	–	V

[1] The characteristics of VDD12 under-voltage 0 and VDD12 under-voltage 1 are the same.

5.7 PLL characteristics

Table 5-7: PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DVDD}	3.3V power supply	–	2.97	3.3	3.63	V
f_{VCO}	VCO frequency	–	400	500	600	MHz
f_{pfd}	Phase-Frequency Detector (PFD) input frequency	–	4	–	8	MHz
t_{LOCK}	Locking time	–	–	–	15	us

5.8 14-bit ADC characteristics

Table 5-8: ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DVDD}	Power supply	–	2.97	3.3	3.63	V
N_R	Resolution	No missing code. Monotonic	14	–	–	bit
F_S	Conversion speed[1]	–	–	–	4	MSPS
V_{AIN}	Input voltage range	–	0	–	V_{DVDD}	V
V_{REF}	Reference voltage	–	1.194	1.2	1.206	V
I_{on}	Operational current	V_{DVDD} = 3.3 V	–	17.1	21	mA
INL	Integral linearity error	–	-3.0	–	3.0	LSB
DNL	Differential linearity	–	-1.0	–	1.0	LSB
E_{OFF}	Offset error[2]	With calibration	-2	–	2	LSB
E_{GAIN}	Gain error[2]	With calibration	-4	–	4	LSB
E_{OFF2}	Channel to channel offset	–	-3	–	3	LSB
E_{GAIN2}	Channel to channel gain error	–	-5	–	5	LSB
T_{COEF}	ADC temperature coefficient with internal reference	–	–	26	–	ppm/°C
t_{setup}	Power-up time	–	–	–	200	us
$ENOB_{DC}$	DC Noise Floor	–	–	12.0	–	bits
SNR	Signal-to-noise ratio	f_{in} = 100 kHz Amp = 0.94 F_S N = 8192	–	75.5	–	dB
THD	Total harmonic distortion		–	-85.0	–	dB
ENOB	Effective number of bits		–	12.2	–	bits
SFDR	Spurious free dynamic range		–	86.0	–	dB
T_{slope}	Degrees C of temperature movement per measure ADC LSB change of the temperature sensor	–	–	1.904	–	°C/LSB
T_{offset}	ADC output at 25 °C of the temperature sensor	–	–	162.138	–	LSB

[1] Sampling time = 110ns, Conversion time = 140ns.

[2] The offset and gain can be automatically calibrated by hardware.

5.9 Analog comparator characteristics

Table 5-9: Comparator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DVDD}	Power supply	–	2.97	3.3	3.63	V
V_{OFFSET}	Offset voltage (Hysteresis voltage=0)	common-mode input voltage = 1.65V	-10	–	10	mV
V_{HYST}	Hysteresis voltage(12mV)	–	–	13	–	mV
	Hysteresis voltage(24mV)	–	–	26	–	mV
	Hysteresis voltage(36mV)	–	–	42	–	mV
t_D	Delay time - comparator response time to PWM shunt down (Asynchronous)	–	–	50	–	ns

5.10 Internal 10-bit DAC characteristics

Table 5-10: DAC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DVDD}	Power supply	–	2.97	3.3	3.63	V
N	resolution	Monotonic	10	–	–	bit
V_{FS}	Full scale value	–	0	–	V_{DVDD}	V
DNL	Differential linearity	–	-0.5	–	0.5	LSB
INL	Integral linearity	–	-1	–	1	LSB
E_{OFF}	Offset error	–	–	5	–	mV
t_{settle}	DAC settling time	Design guarantee	–	–	1	us

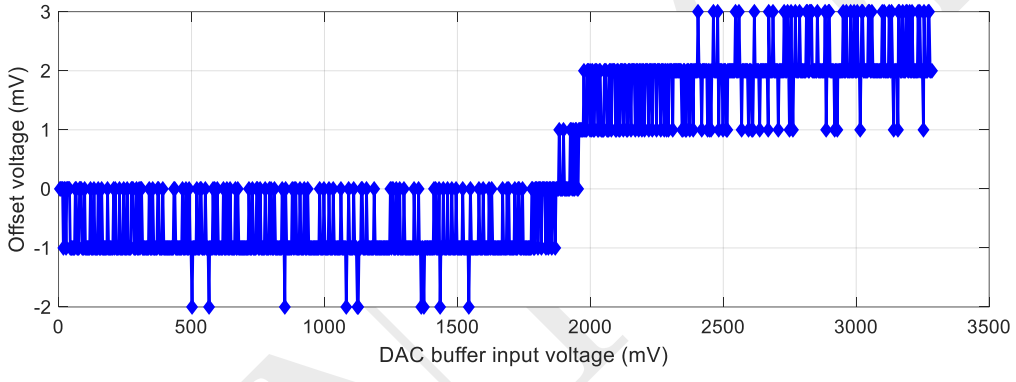
[1] The DAC is used to generate a static voltage as a threshold for the comparator and does not guarantee the performance of the waveform produced by dynamically changing the code value.

5.11 DAC buffer characteristics

Table 5-11: DAC buffer characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DVDD}	Power supply	–	2.97	3.3	3.63	V
V_{OUT}	Output voltage range	–	0.3	–	V_{DVDD} - 0.3	V
t_{settle}	Settling time	Design guarantee	–	1	–	us
E_{OFF}	Offset error	–	–	3	–	mV
C_L	Capacitor load	–	–	–	50	pF
R_L	Resistive load	–	1M	–	–	Ω

Figure 5-3: DAC buffer offset voltage vs. input voltage



5.12 Flash memory characteristics

Table 5-12: Flash memory characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
t_{read}	Read access time	–	40	–	ns
t_{PROG}	Word (32-bit) program time	–	8	10	us
t_{SE}	Sector erase time	–	0.8	4	ms
t_{BE}	Chip erase time	–	8	10	ms
N_{cycle}	Endurance (erase/program cycle)	T_J = 85 °C	100,000	–	cycles
$t_{retention}$	Data retention duration	T_J = 85 °C	10	–	years

5.13 Electrical sensitivity characteristics

Table 5-13: ESD absolute maximum ratings

Symbol	Parameter	Conditions		Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human Body Model)	Ambient temperature T_A = 25 °C		1250	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charge Device Model)	Ambient temperature T_A = 25 °C	–	750	V
			Corner Pin	750	V

Table 5-14: Electrical sensitivities

Symbol	Parameter	Conditions	Max	Unit
LU	Static latch-up	Ambient temperature T_A = 125 °C V_{VCAP12} = 1.32 V， V_{DVDD}=3.63 V， $V_{VBOOT\_W/U/V}$ = 20 V， V_{VDDG} = 20 V， V_{BUS} = 200 V	200	mA
		Ambient temperature T_A = 25 °C V_{VCAP12} = 1.32 V， V_{DVDD} = 3.63 V， $V_{VBOOT\_W/U/V}$ = 20 V， V_{VDDG} = 20 V， V_{BUS} = 200 V	200	mA

5.14 Moisture sensitivity characteristics

Table 5-15: Moisture sensitivity characteristic

Symbol	Parameter	Conditions	Level	Unit
MSL	Moisture sensitivity level	–	Level 3	–

5.15 Thermal resistance characteristics

Table 5-16: Thermal resistance characteristics (HFBP39 package)

Symbol	Parameter	Conditions	Typ	Unit
θ_{JC}	Junction-to-case thermal resistance	–	TBD	°C/W
θ_{JA}	Junction-to-ambient thermal resistance	Single layer PCB PCB Copper content=20%	TBD	°C/W
		4-layer PCB PCB Copper content (Top layer = 20%, Second/Third layer = 100%, Bottom layer = 5%)	TBD	°C/W

[1] The size of PCB test board is 76.2mm x 114.3mm x 1.6mm.

5.16 Gate driver characteristics

Table 5-17: Gate driver characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DDGUVT}	VDDG under voltage lock out trigger	–	7.9	8.9	9.9	V
V_{DDGUVH}	VDDG under voltage lock out hysteresis	–	–	1	–	V
V_{BSUVT}	VBS under voltage lock out trigger	–	7.9	8.9	9.9	V
V_{BSUVH}	VBS under voltage lock out hysteresis	–	–	1	–	V
I_{LK}	High side leakage current	–	–	–	1	uA
I_{QBS}	Quiescent BS current	–	–	50	120	uA
I_{QVDDG}	Quiescent VDDG current	–	–	402	–	uA
R_{BS}	Bootstrap resistance	–	–	100	–	Ω
$V_{DDG(BR)}$	Max VDDG Breakdown Voltage	–	–	22	–	V
$V_{BS(BR)}$	Max VBOOT-VPX Breakdown Voltage	–	–	22	–	V

5.17 Integrated MOS characteristics

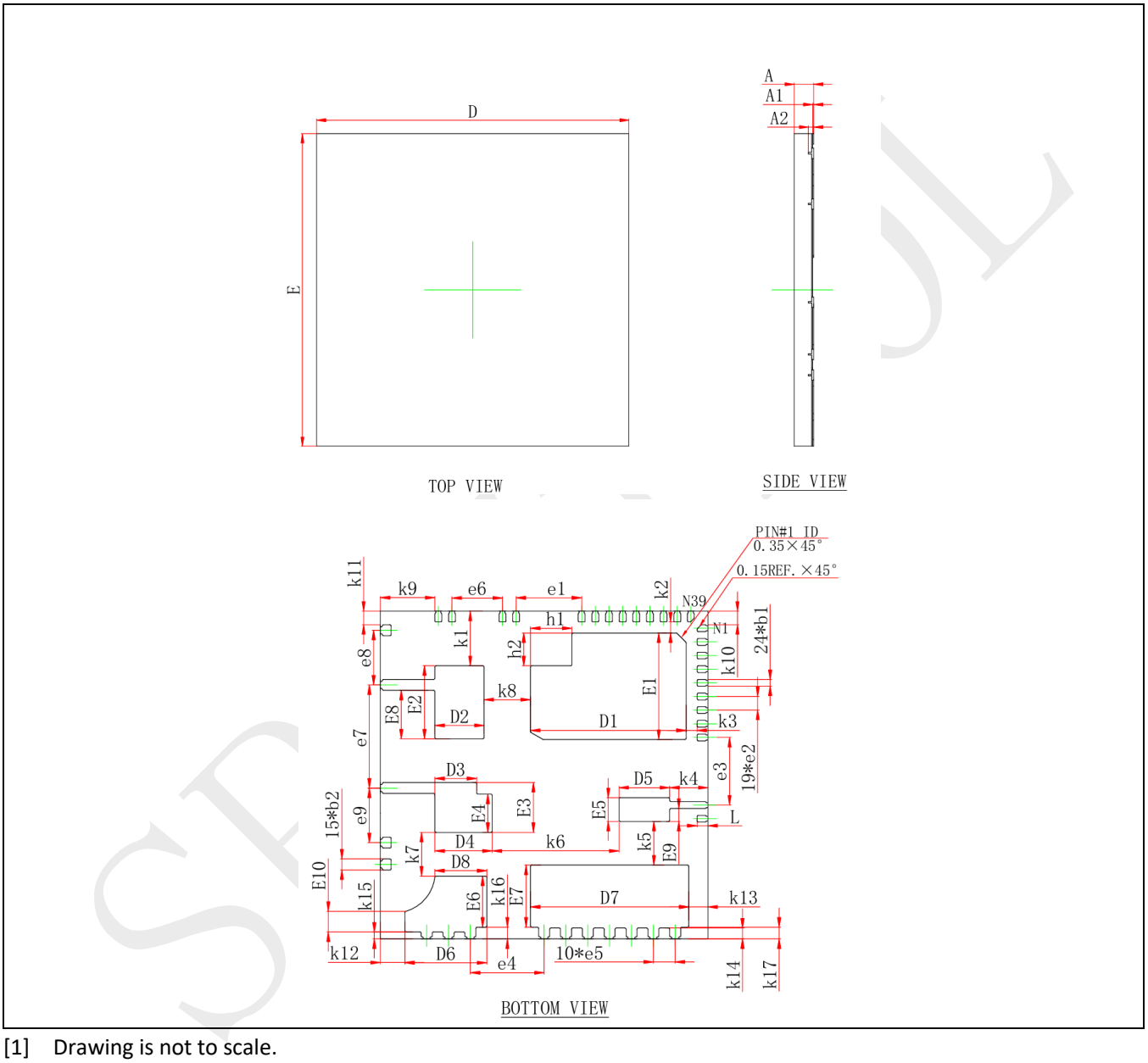
Table 5-18: Integrated MOS characteristics

Symbol	Definition	Condition	Min	Type	Max	Units
$V_{DS(BR)}$	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250uA	–	650	–	V
R_{on}	Drain-Source On-State Resistance	V_{GS} = 15V, I_D = 0.5A	–	1.9	2.5	Ω
V_{th}	Threshold Voltage	V_{GS} = V_{DS}, I_D = 250uA	–	4.0	–	V
I_{out_dc}	Device output current (DC)	–	–	2	–	A

6 Package information

6.1 HFBP39

Figure 6-1: HFBP39, 12 x 12 x 0.75 mm³ low-profile quad flat package outline



[1] Drawing is not to scale.

Table 6-1: HFBP39, 12 x 12 x 0.75 mm³ low-profile quad flat package mechanical data

Symbol	Dimensions in Millimeters(mm)			Dimensions in inches(in)		
	Min.	Nor.	Max.	Min.	Nor.	Max.
A	0.7	0.75	0.8	0.028	0.03	0.031
A1	0	–	0.05	0	–	0.002
A2	0.203REF.			0.008REF.		
D	12.000BSC.			0.472BSC.		
E	12.000BSC.			0.472BSC.		
b1	0.2	0.25	0.3	0.008	0.01	0.012
b2	0.35	0.4	0.45	0.014	0.016	0.018
D1	5.6	5.7	5.8	0.22	0.224	0.228
D2	1.7	1.8	1.9	0.067	0.071	0.075
D3	1.43	1.53	1.63	0.056	0.06	0.064
D4	2	2.1	2.2	0.079	0.083	0.087
D5	1.76	1.86	1.96	0.069	0.073	0.077
D6	2.9	3	3.1	0.114	0.118	0.122
D7	5.7	5.8	5.9	0.224	0.228	0.232
D8	1.900REF.			0.075REF.		
E1	3.8	3.9	4	0.15	0.154	0.157
E2	2.575	2.675	2.775	0.101	0.105	0.109
E3	1.725	1.825	1.925	0.068	0.072	0.076
E4	1.3	1.4	1.5	0.051	0.055	0.059
E5	0.77	0.87	0.97	0.03	0.034	0.038
E6	1.77	1.87	1.97	0.07	0.074	0.078
E7	2.17	2.27	2.37	0.085	0.089	0.093
E8	1.675	1.775	1.875	0.066	0.070	0.074
E9	0.375	0.475	0.575	0.015	0.019	0.023
E10	0.750REF.			0.030REF.		
e1	2.400BSC.			0.094BSC.		
e2	0.500BSC.			0.020BSC.		
e3	2.475BSC.			0.974BSC.		
e4	2.700BSC.			0.106BSC.		
e5	0.800BSC.			0.031BSC.		
e6	1.850BSC.			0.728BSC.		
e7	3.775BSC.			0.149BSC.		
e8	2.000BSC.			0.079BSC.		
e9	2.000BSC.			0.079BSC.		
L	0.35	0.4	0.45	0.014	0.016	0.018
k1	2.000REF.			0.079REF.		
k2	0.400REF.			0.016REF.		
k3	0.400REF.			0.016REF.		
k4	1.400REF.			0.055REF.		

Symbol	Dimensions in Millimeters(mm)			Dimensions in inches(in)		
	Min.	Nor.	Max.	Min.	Nor.	Max.
k5		1.600REF.			0.063REF.	
k6		4.640REF.			0.183REF.	
k7		1.600REF.			0.063REF.	
k8		1.700REF.			0.067REF.	
k9		2.000REF.			0.079REF.	
k10		0.500REF.			0.020REF.	
k11		0.500REF.			0.020REF.	
k12		0.900REF.			0.035REF.	
k13		0.700REF.			0.028REF.	
k14		0.250REF.			0.010REF.	
k15		0.400REF.			0.016REF.	
k16		0.430REF.			0.017REF.	
k17		0.430REF.			0.017REF.	
h1	1.415	1.515	1.615	0.056	0.06	0.064
h2	1.1	1.2	1.3	0.043	0.047	0.051

7 PCB Layout and Routing Recommendations

- SW trace routing should follow the minimization principle: maintain the shortest path and maximum allowable width to optimize EMI performance.
- To achieve the lowest trace impedance, widen the following GND pin traces as much as possible:
  - GND traces between the DVDD capacitor and the GND pin.
  - GND traces between the VDDG bypass capacitor and the GND pin.
  - GND traces between the VCAP12A/B bypass capacitors and the GND pin.
- Pre-driver routing requirements:
  - Implement star grounding to eliminate common-mode interference.
  - The interconnection traces between the VBOOT capacitor and the VPX pin should be made as wide and short as possible to ensure minimized impedance.

8 Ordering information

Table 8-1: Ordering information

Ordering Code	Flash	SRAM	CPU f_{MAX}	Package	Temperature Range	SPQ[1]	Packing
SPM1173ZAPI39	64KB	32KB	100MHz	HFBP39 (12 × 12 × 0.75 mm^3)	Industrial -40 °C to +125 °C	1680	Tray

[1] SPQ = Standard Pack Quantity.

8.1 Rule of ordering code

Figure 8-1: Rule of ordering code